



# International Journal of Innovative Research in Science Engineering and Technology (IJIRSET)

*(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)*



**Impact Factor: 9.935**

**Volume 15, Issue 5, May 2026**

# A Novel Approach for AMBA - AXI Protocol Verification for Bus Integration using SV System

Raja M, Dr. E. Sathishkumar

P.G. Student, Department of Electronics and Communication Engineering, Gnanamani College of Technology,  
Namakkal, India

Associate Professor, Department of Electronics and Communication Engineering, Gnanamani College of Technology,  
Namakkal, India

**ABSTRACT:** Highly developed Microcontroller Bus Architecture Advanced extensible Interface (AMBA AXI) provided by the ARM supports the high performance and high frequency system design. The System on Chip (SOC) Integration design needs to meet the low latency and high bandwidth challenges. The complex bridges are necessary when high frequency operations are carried out and there is a need for the interface which meets the requirement for the wide range of the applications, all such requirements without the complex bridges are provided by the AMBA AXI. The verification of such a bus protocol required to make the SOC integration most robust one. System Verilog based verification methodology provides the systematic way of verifying such a SOC to make it as a most reliable one. Also, SV based assertion makes the checking all the protocols specification easier at the verification stage. In the present system, the general design and verification methodologies for the AXI-Bus and Memory interface for SOC integration is proposed. Verilog based memory and AXI design being done using Verilog HDL and design challenges are discussed. The proposed design implementation supports single and burst based data transfers. The AXI protocol provides the dedicated channels for memory read and write operations. In this work, single master and single slave communication using AXI protocol with 32-bit SARM are designed and implemented. The System Verilog based verification environment is setup and used for the verification IP development. And SV Assertion based verification is being done to thoroughly check the AXI protocol functionality.

**KEYWORDS:** AMBA (Advanced Microcontroller Bus Architecture), AXI Protocol

## I. INTRODUCTION

The AMBA AXI's highly advanced features enable its use in almost all highspeed SOC and NOC integration design applications. Since AXI's vast specification makes the design of the system complex and involves numerous challenges. The design of such a complex system leads to developing a generalized predesign called Intellectual property (IP), which can be reused for different applications. System Verilog (SV) is the verification language which provides the various construct to well verify the intended design with all verification aspects. It provides the high-level verification constructs and verification environment based on the object-oriented the object-oriented programming (OOPs). The verification of SOC integration are well implemented using these constructs, the verification IP developed are reusable. AMBA AXI (Advanced Microcontroller Bus Architecture, Advanced extensible Interface) is a high-performance, high-frequency on-chip communication protocol that is part of the Arm AMBA specification. It supports simultaneous read and write operations, multiple outstanding transactions, and out-of-order data, making it suitable for high-bandwidth, low-latency system designs. Key features include five unidirectional channels, flexible timing, and support for unaligned data transfers.

## II. LITERATURE SURVEY

The Static Random Access Memory SRAM Controller with AXI is intended to improve the read/write memory access time and internal connectivity of the semiconductor. Static random-access memory is used by one shared bus, with the aid of Advanced Microcontroller Bus Architecture AMBA. Utilizing System Verilog technology, the system's functionality of SRAM with AXI is ensured. The SRAM, which is designed is reconfigurable to different memory and AXI data and address widths. All of the modules in SV's basic test framework are hardwired to one another, which limits reusability. Industrial standard utilizes the Universal Verification Methodology UVM as its standard verification

methodology. It reflects quick developments that allow the user to design reliable and reusable test bench components and verification intellectual property. Advanced Microcontroller Bus Architecture supports high-speed on-chip communication. AMBA protocols are Advanced High-performance Bus, Advanced Peripheral Bus, and Advanced extensible Interface. Serial Peripheral Interface is a simple, full duplex serial protocol. Amidst the modern technological landscape, microelectronics has assumed unparalleled significance in individuals' daily lives. The heightened demand for these components, coupled with their limited availability, imposes constraints on production timelines and elevates final product failure rates. Consequently, there is a critical need for methodologies that enhance the efficiency and effectiveness of hardware design and verification, where the latter has become a predominant cost in the overall design process. Addressing this challenge, the Advanced Microcontroller Bus Architecture (AMBA) emerges as an open-standard on-chip interface interconnect.

### III. METHODOLOGY

The Advanced Micro controller Bus Architecture (AMBA) bus protocols is a set of interconnect specifications from ARM that standardizes on chip communication mechanisms between various functional blocks (or IP) for building high performance SOC designs. These designs typically have one or more micro controllers or microprocessors along with several other components—internal memory or external memory bridge, DSP, DMA, accelerators and various other peripherals like USB, UART, PCIE, I2C etc—all integrated on a single chip. The primary motivation of AMBA protocols is to have a standard and efficient way to interconnecting these blocks with re-use across multiple designs.

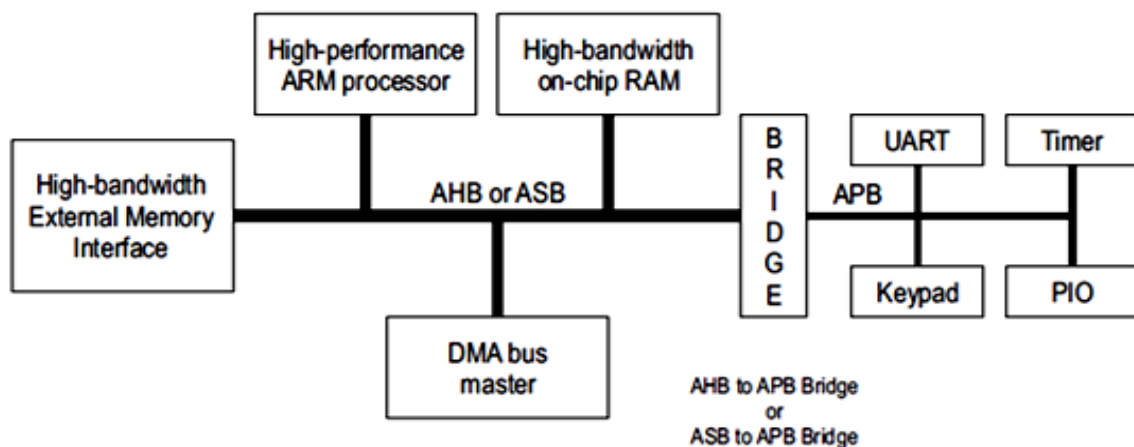


Figure3.1. AMBA bus architecture

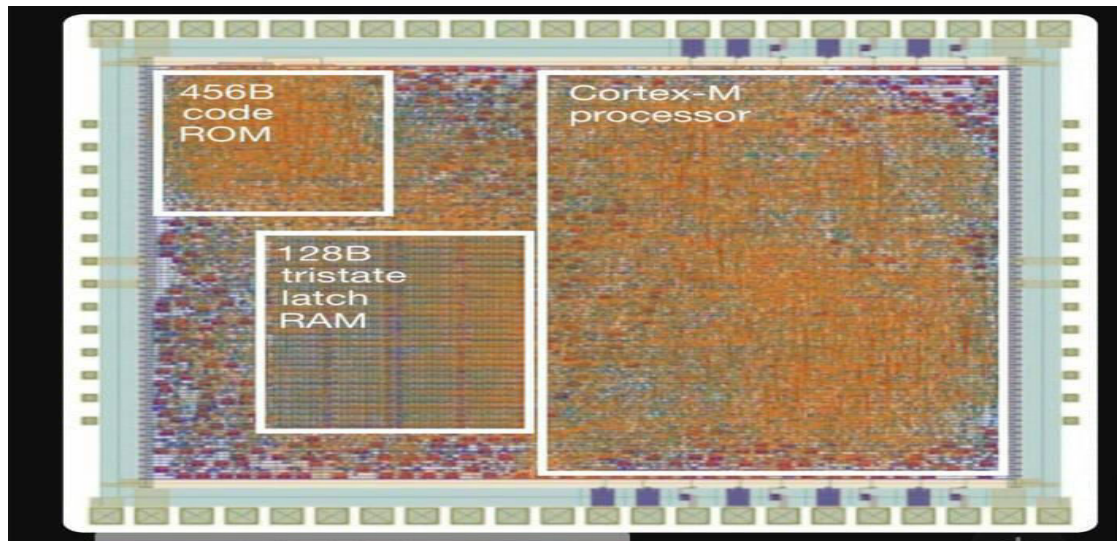
The interconnect could be a custom crossbar or a switch design or even an off the shelf NOC (Network on Chip) IP that supports multiple AXI masters and slaves. The AXI interconnect helps in scaling up connectivity for number of agents compared to previous AHB/ASB bus. An AXI to APB bridge on one of the slave port is normally used to bridge communications to a set of peripherals shared on an APB bus. Further evolution happened in the era of mobile and smartphones with SOCs having dual/quad/octa core processors with shared caches integrated and the need for hardware managed coherency across the memory subsystem. This led to the introduction of ACE (AXI Coherency Protocol Extension) in AMBA revision 4. Lastly, in the current era of heterogeneous computing for HPC and data center markets, the integration trend continues with increasing number of processor cores along with several heterogeneous computing elements like GPU, DSP, FPGAs, memory controllers and IO sub systems. In 2013, AMBA 5 introduced the CHI (Coherent Hub Interconnect) protocol as a re-design of the AXI/ACE protocol. The signal based AXI/ACE protocol was replaced with the new packet based CHI layered protocol that can scale very well for near term future. AXI is burst based protocol and has 5 independent dedicated channels for the write and read operation between the master and slave. Read operation is carried out using read address and read data channels whereas write operation is carried out using write address, write data and write response channels. The address channels carry the read and write

related control information. AXI protocol supports the issue of the address information before the actual data transfer, also it issues the multiple outstanding and out-of-order completion transactions.

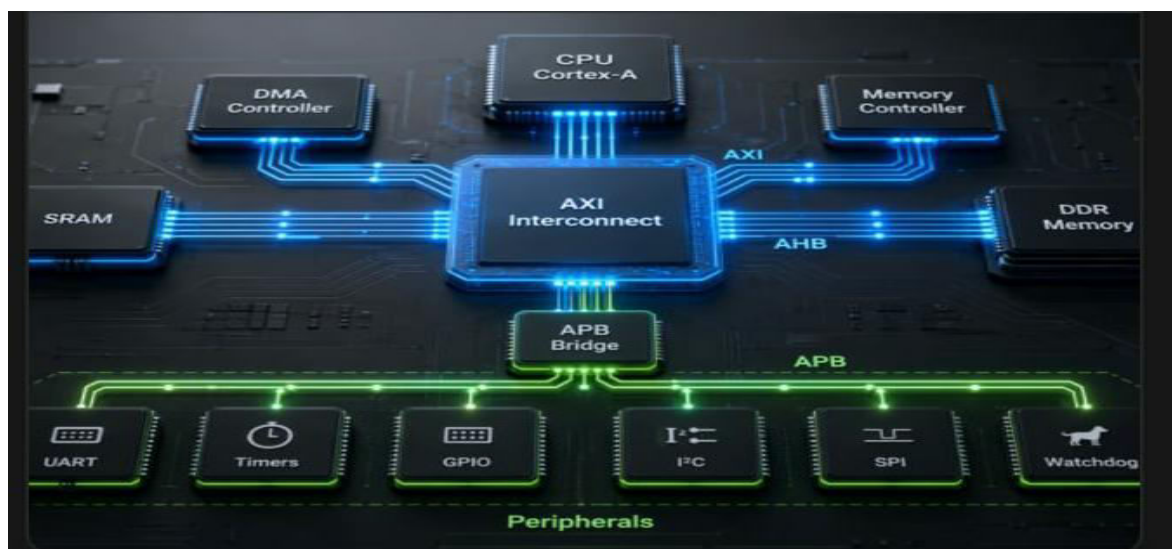
#### IV. EXPERIMENTAL RESULTS

**APB :** The *Advanced Peripheral Bus (APB)* is used for connecting low bandwidth peripherals. It is a simple non-pipelined protocol that can be used to communicate (read or write) from a bridge/master to a number of slaves through the shared bus. The reads and writes shares the same set of signals and no burst data transfers are supported. The latest spec (APB 2.0) is available on **ARM website here** and is a relatively easy protocol to learn.

**AHB:** The *Advanced High-performance Bus (AHB)* is used for connecting components that need higher bandwidth on a shared bus. These could be a internal memory or an external memory interface, DMA , DSP etc but the shared bus would limit the number of agents. Similar to APB, this is a shared bus protocol for multiple masters and slaves, but higher bandwidth is possible through burst data transfers.



(a)



(b)

### V. CONCLUSION

The SOC integration based on AMBA AXI BUS protocol involves complexity, which induces numerous challenges design implementation and integration phases. In this paper the verification IP based on the AXI protocol is being developed and AXI based single master-slave read write transaction is carried out. The verification IP is developed based on the systematic approach based on the system Verilog verification environment. This kind of verification environment provides the plat form for strategizing and developing the fully coverage driven verification IPs for any complex designs. This work can be extended to burst based transactions and make the integrated system works perfectly. So, SV based verification strategies can be adopted for any complex SOC Integration verification.

### REFERENCES

- [1] Shaila C K; I.Thusnavis Bella Mary; Divya P.S.; Shylu Sam D S; G.Yaswanthi; G Manoj “Design & Verification of Reconfigurable SRAM Controller with AMBA AXI Protocol Interface for Automobile Application” IEEE - 2025 2nd International Conference on Trends in Engineering Systems and Technologies (ICTEST)
- [2] Dr. A. Navaneetha\*1, K. Sidhisree\*2, Nihanth Viswanadhapalli\*3, Anumala Abhinav\*4 \*1Assistant Professor, Department Of ECE, Mahatma Gandhi Institute Of Technology “COMPARATIVE ANALYSIS OF AMBA PROTOCOLS WITH SPI” – IJRMETS Volume:07/Issue:04/April-2025
- [3] Lakshmi Sirisha B, Sambasivarao Nakkala, “Design and Verification of AMBA AXI Protocol” semantic scholar - DOI:10.1109/ICECCC61767.2024.10593998
- [4] Harish T L , Dr. M C Chandrashekhar , Dr. Eshwarappa M N “Design of AXI4 Slave Device Using VERILOG” IJSDR - Vol.8, Issue 6, page no.1474 - 1479, June-2023
- [5] Vishwas B R, Dr. Sowmya K B “Design and Implementation of Advanced Extensible Interface using Verilog” IJRASET- 2023-08-22 ISSN : 2321-9653
- [6] Nagendrareddy S1, Jagadeesha kolour K2, Basarkod P I3 “Verification of AXI IP Core(Protocol) using System Verilog” IRJET - Volume: 06 Issue: 05 | May 2019
- [7] Rashmi Samanth, Subramanya G. Nayak “Design and SV Based Verification of AMBA AXI Protocol for SOC Integration” IJRTE - ISSN: 2277-3878 (Online), Volume-8 Issue-2, July 2019
- [8] V.N.M.Brahmanandam K, Choragudi Monohar “Design of Burst Based Transactions in AMBAAXI Protocol for SoC Integration” International Journal of Scientific & Engineering Research Volume 3, Issue 7, July-2012



INTERNATIONAL  
STANDARD  
SERIAL  
NUMBER  
INDIA



# INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 9940 572 462  6381 907 438  [ijirset@gmail.com](mailto:ijirset@gmail.com)



[www.ijirset.com](http://www.ijirset.com)

Scan to save the contact details